PhD Position: Perennial hardware accelerators generation

The MOCS team at Lab-STICC ENSTA-Bretagne is searching for a young, motivated and skilled PhD researcher with a strong background in computer engineering.

Position: PhD student
Duration: 36 months *starting date:* September/October 2018
Requirements: Master + European citizen
Where: MOCS team at Lab-STICC ENSTA-Bretagne, Brest
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About Lab-STICC ENSTA-Bretagne

ENSTA Bretagne was founded in 1971 and is a multidisciplinary engineering institute under the auspices of the French Defence Ministry (DGA). ENSTA Bretagne has established itself in the field of IT oriented research, thought its laboratory Lab-STICC (UMR 6285), standing for ”Information and Communication Science and Technology Laboratory. Lab-STICC is a French National Centre for Scientific Research (CNRS) mixed unit shared with two universities and two other engineering institutes.
Lab-STICC’s focus can be summed up in the following motto: COMMUNICATE and DECIDE « from sensor to knowledge » standing for bringing solutions for physical layers at radio- frequency level, designing data transmission and management systems based on advances in both algorithmic and micro-electronic fields, and analysing information to deliver knowledge to final users.
Lab-STICC ENSTA Bretagne has been developing several tools that perform system level design and verification (OBP, http://www.obpcdl.org/), high-level synthesis (Morphose), and low-level reconfigurable architecture modelling & design kit (Madeo), that are currently being retargeted to security concerns.

Context

The search for performance (computing power, low consumption, controlled marginal cost, adaptability to changing contexts) motivates the use of reconfigurable technologies such as FPGAs. On the other hand, these technologies suffer from a rapid obsolescence, making them hardly compatible with long-term operational capabilities. This thesis aims to solve this weakness by an overlay approach.

Research Topic

The thesis addresses the sustainability of methods of material developments in a defence context, which is characterized by a time of operational maintenance (MCO) much longer than the typical challenges of civilian. The main issues is fighting against material obsolescence, with no compromise on performances, and avoiding the preventive storage of extra devices, intended to replace faulty elements over time. This requires the ability to port any application on some changing underlying supports, while offering a behaviour / characteristics conformity, so that different generations of devices can co-operate in a transparent manner.

This thesis focuses on FPGA, which shows the appropriate properties for military and / or spatial use (hardened version, excellent cost / performance ratio, reasonable design time, etc.). Unfortunately, FPGAs do not have standardized programming models as found in the software world (runtime-independent programming languages, multi-target compilers, standardized instruction sets). As a consequence neither sources nor binaries are portable from one target to another. The strong coupling between hardware target and compilation and synthesis tools, as well as the lack of virtualization (and even more so on heterogeneous architectures) make "Platform As a Service" (PAaS) approaches impracticable. PAaS / cloud approaches traditionally offer full resource exploitation, multi-tenant sharing, load balancing, task migration, and more, which are little or not present in the FPGA context [1, 2 3]. A partial solution to the problem is provided by the notion of overlay [4,5], which in contrast often leads to degraded performance [6,7], compared to a bare implementation.

The challenge is therefore to obtain effective (FPGA computation acceleration, full use of resources) and adaptable (remotely triggered evolutions) solutions for the different generations to interoperate in a transparent manner. Thus the proposed approach must ensure that the addition, replacement, or removal of devices will be possible without heavy impact.

The thesis will firstly sweep all the alternatives in the state of the art that ensure the durability of material developments. A sensitive issue is the combination of backward compatibility of new devices (ability to work with older devices) with upward compatibility of devices already in circulation (ability to ignore future incompatible versions). For this, the PhD student will rely on a joint expertise, coming from the respective laboratories of the two co-supervisors:

• The first tool (Augh), developed at TIMA, is a high level synthesizer (C to VHDL), that decorates the produced architecture in order to allow controllability. Context extraction is thus made possible at runtime for task migration.
• The second solution (Biniou) is target virtualization via an overlay mechanism (FPGA over FPGA), along with its programming, deployment, and exploitation environments. Only one programming framework is considered, but performance is highly dependent on the overlay.

The thesis aims to converge towards a heterogeneous, coarse overlay architecture. This architecture will be evaluated for a given application class (and ideally representative of defence problems). Ultimately, the automatic extraction of critical parameters for the design of the overlay from a set of reference applications will provide an end-to-end solution.

References:

Internal References

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PhD thesis

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[T2] Théotime Bollengier, « Du Prototypage à l'Exploitation d'Overlays FPGA », Jan. 2018 Thèse ENSTA Bretagne

External References

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